



January 12, 2004

To: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Daavis Avenue
Poughkeepsie, N.Y. 12603

Subject: | Serial No. 10/685,872 10/15/03 |

M.S. Lin

POST PASSIVATION INTERCONNECTION
SCHEMES ON TOP OF THE IC CHIPS

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation
In An Application.

The following Patents and/or Publications are submitted to
comply with the duty of disclosure under CFR 1.97-1.99 and
37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being
deposited with the United States Postal Service as first class
mail in an envelope addressed to: Commissioner of Patents and
Trademarks, Washington, D.C. 20231, on January 27, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date

A handwritten signature of "SBA" followed by the date "1/27/04".

U.S. Patent 6,383,916 to Lin, "Top Layers of Metal for High Performance IC's," discloses a method of closely interconnecting integrated circuits contained within a semiconductor wafer to electrical circuits surrounding the wafer.

Multichip Module Technologies and Alternatives: the basics, Copyright 1993 by Van Nostrand Reinhold, pp. 755 and 757, shows a Cu bump used for connecting a chip to an active driver substrate.

U.S. Patent 6,495,442 to Lin et al., "Post Passivation Interconnection Schemes on Top of the IC Chips," discloses a method for the creation of interconnect lines.

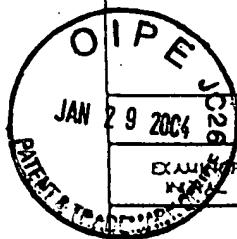
U.S. Patent 6,303,423 to Lin, "Method for Forming High Performance System-On-Chip Using Post Passivation Process," discusses creating high quality electrical components, such as inductors, capacitors or resistors, on a layer of passivation or on the surface of a thick layer of polymer.

MSL98-002CCC-CIP, serial number 10/154,662, filed on May 24, 2002, "Top Layers of Metal for High Performance IC's," discusses the manufacturing of high performance Integrated Circuit (IC's).

Sincerely,



Stephen B. Ackerman, Reg. #37761



Form PTO-1449

**INFORMATION DISCLOSURE CITATION
IN AN APPLICATION**

(Use several sheets if necessary)

Doctor Number (Optional)

MEG-02-015

Appleson Number

10/685, 872

Location

M.S. Lin

Filing Date

10/15/03

Group Art Unit

JAN

JAN 29 2004

U. S. PATENT DOCUMENTS

FOREIGN PATENT DOCUMENTS

OTHER DOCUMENTS (including Author, Title, Date, Portion or Pages, Etc.)

- Multichip Module Technologies and Alternatives: the basics
Copyright 1993 by Van Nostrand Reinhold pp. 755 and 757.
 - MSL 98-002 CCC-CIP, serial number 10/154,662,
filed 5/24/02, "Top Layers of Metal for High Performance
IC's".

EXAMINER

DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.